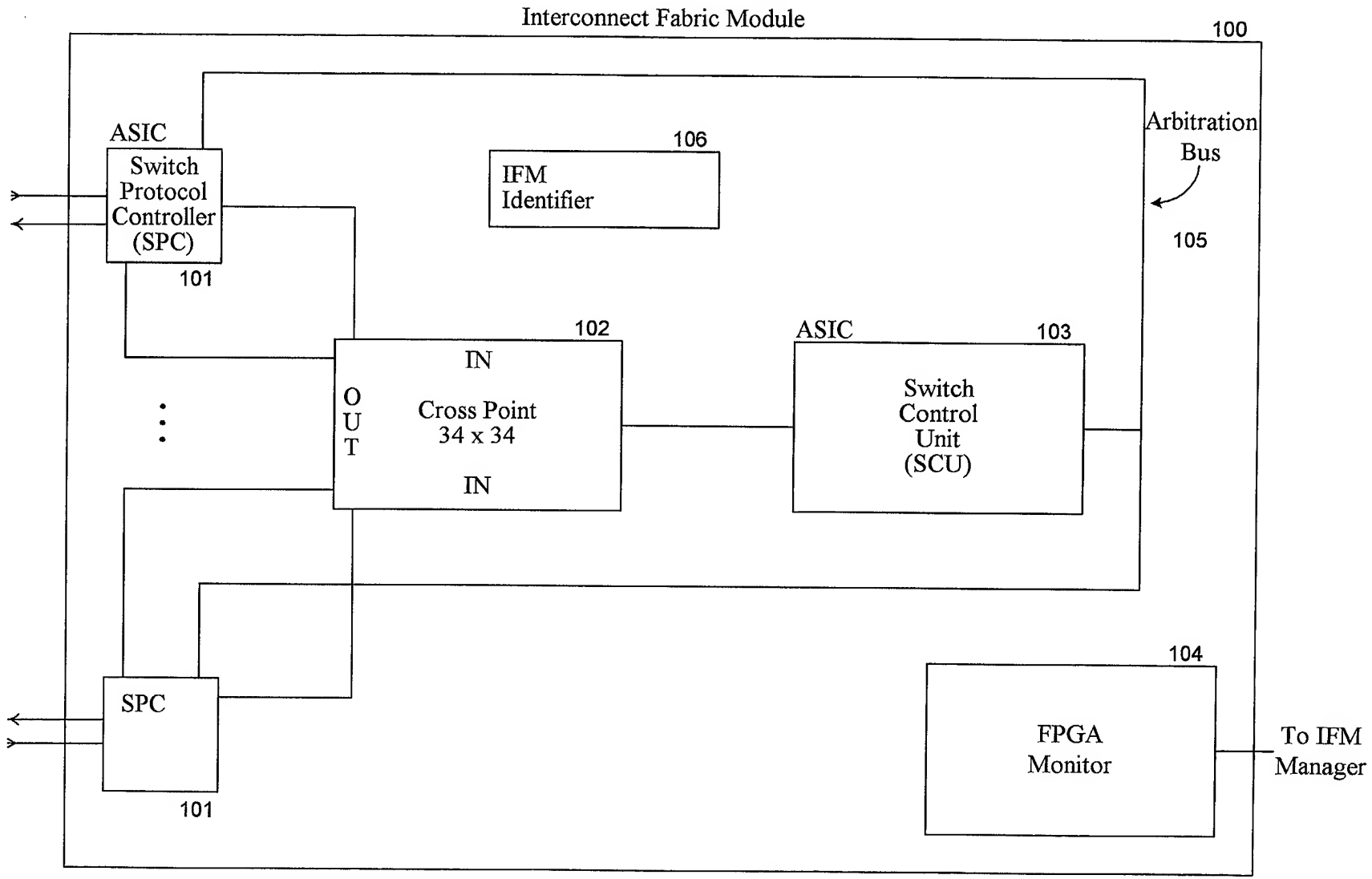

Interconnect Fabric Module
100
ASIC
Switch Protocol Controller (SPC)
101
106
IFM Identifier
Arbitration Bus
105
102
IN
OUT
Cross Point 34 x 34
IN
ASIC
103
Switch Control Unit (SCU)
SPC
101
104
FPGA Monitor
To IFM Manager

Fig. 1

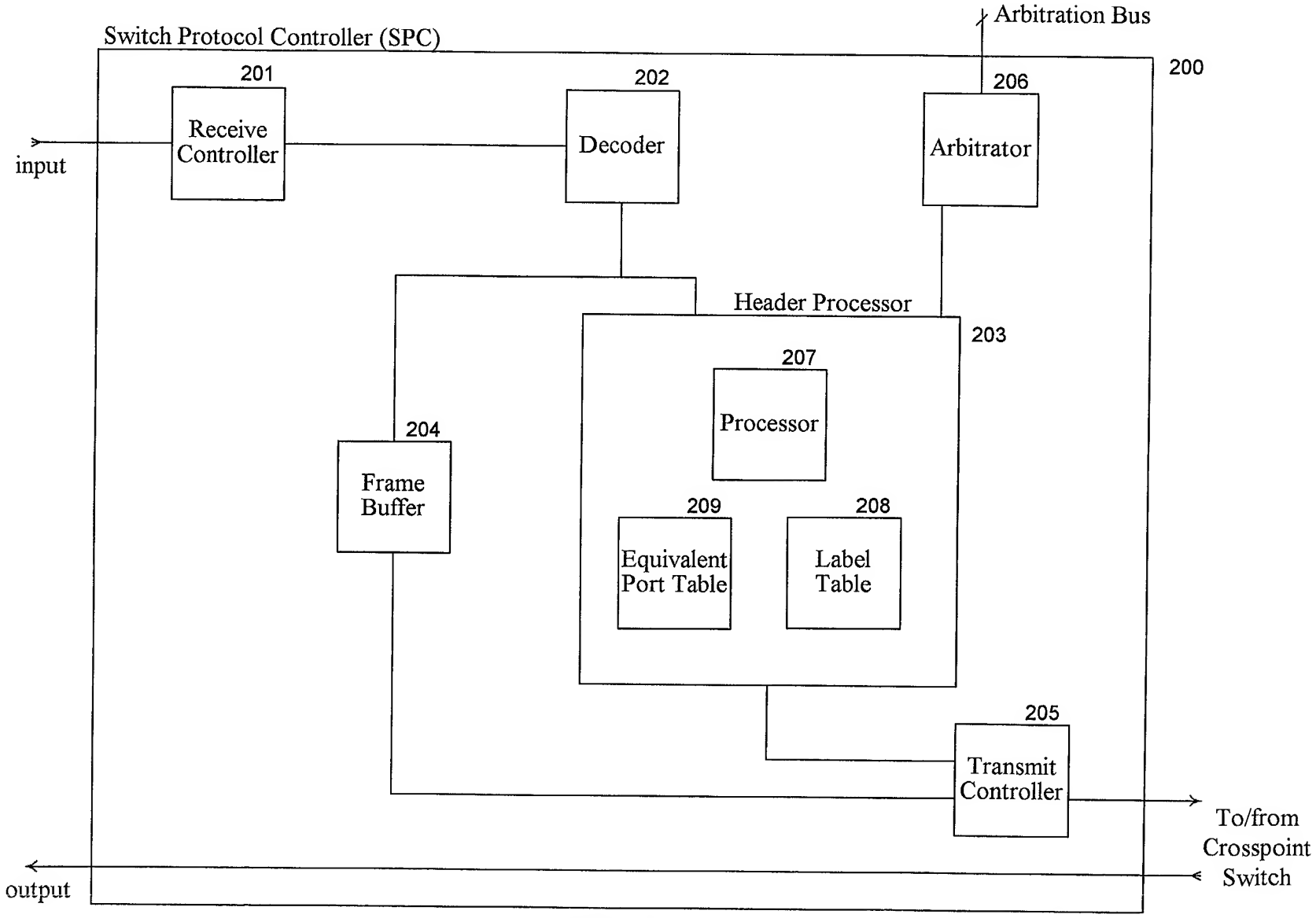

Arbitration Bus
Switch Protocol Controller (SPC)
200
201
Receive Controller
202
Decoder
206
Arbitrator
input
Header Processor
203
207
Processor
204
Frame Buffer
209
Equivalent Port Table
208
Label Table
205
Transmit Controller
To/from Crosspoint Switch
output

Fig. 2

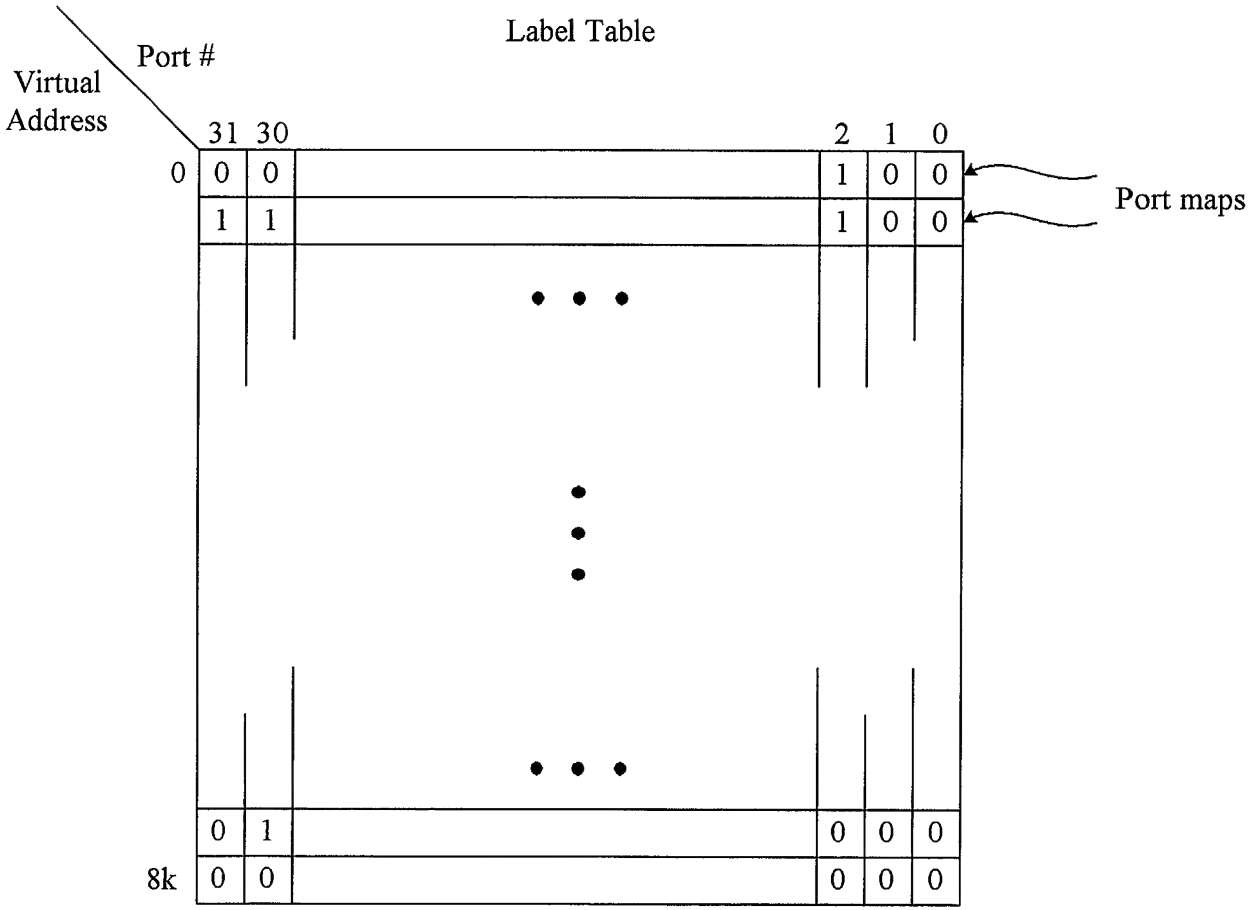

Label Table
Port #
Virtual Address
31 30
2 1 0
0
0 0 1 0 0
1 1 1 0 0
Port maps
0 1 0 0 0
8k
0 0 0 0 0

Fig. 3

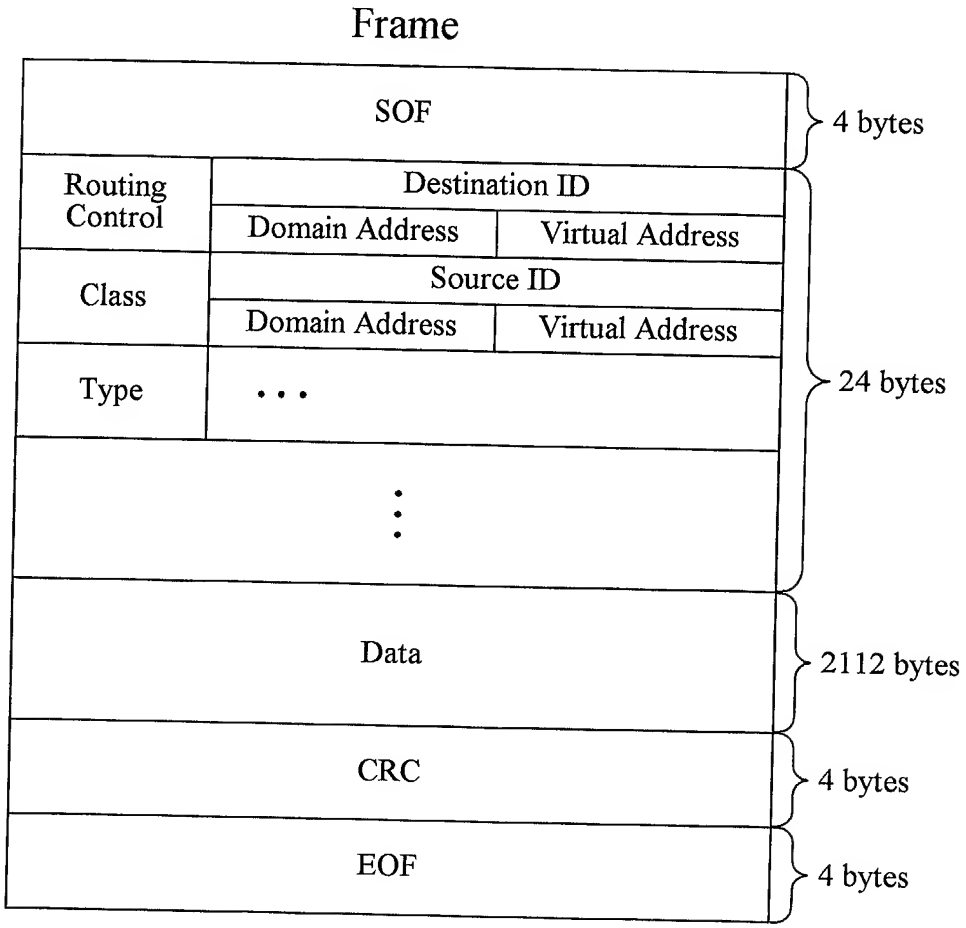

Frame
SOF
4 bytes
Routing Control
Destination ID
Domain Address
Virtual Address
Class
Source ID
Domain Address
Virtual Address
Type
• • •
24 bytes
Data
2112 bytes
CRC
4 bytes
EOF
4 bytes

Fig. 4

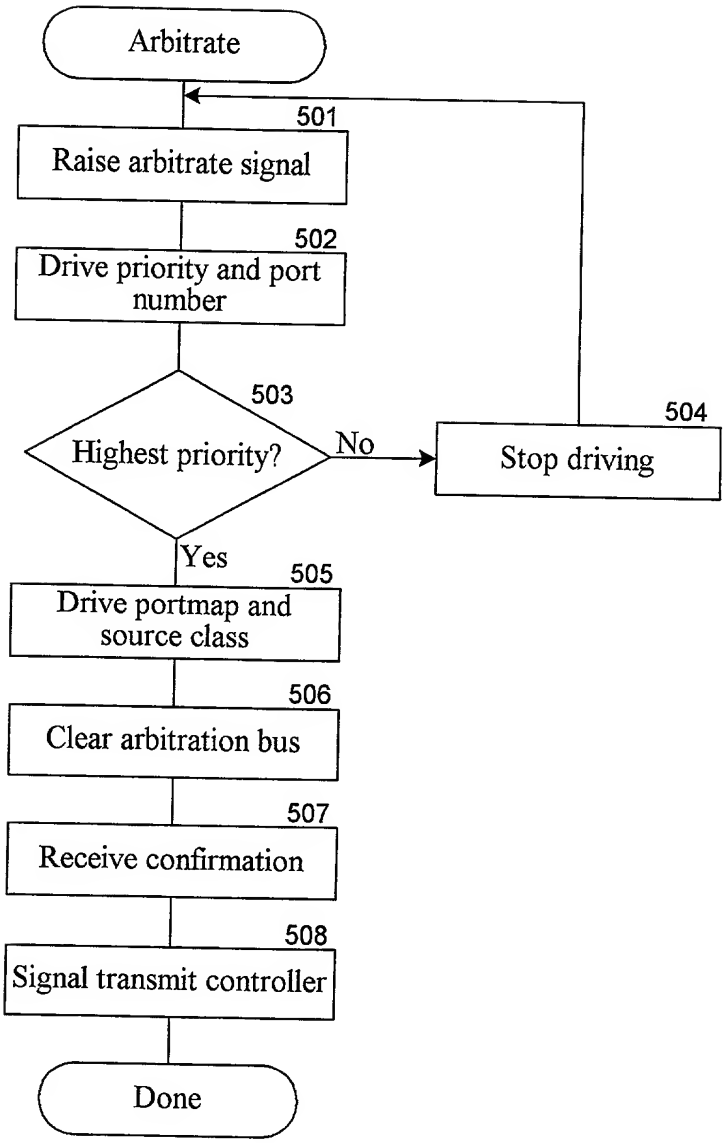

Arbitrate
501
Raise arbitrate signal
502
Drive priority and port number
503
Highest priority?
No
504
Stop driving
Yes
505
Drive portmap and source class
506
Clear arbitration bus
507
Receive confirmation
508
Signal transmit controller
Done

Fig. 5

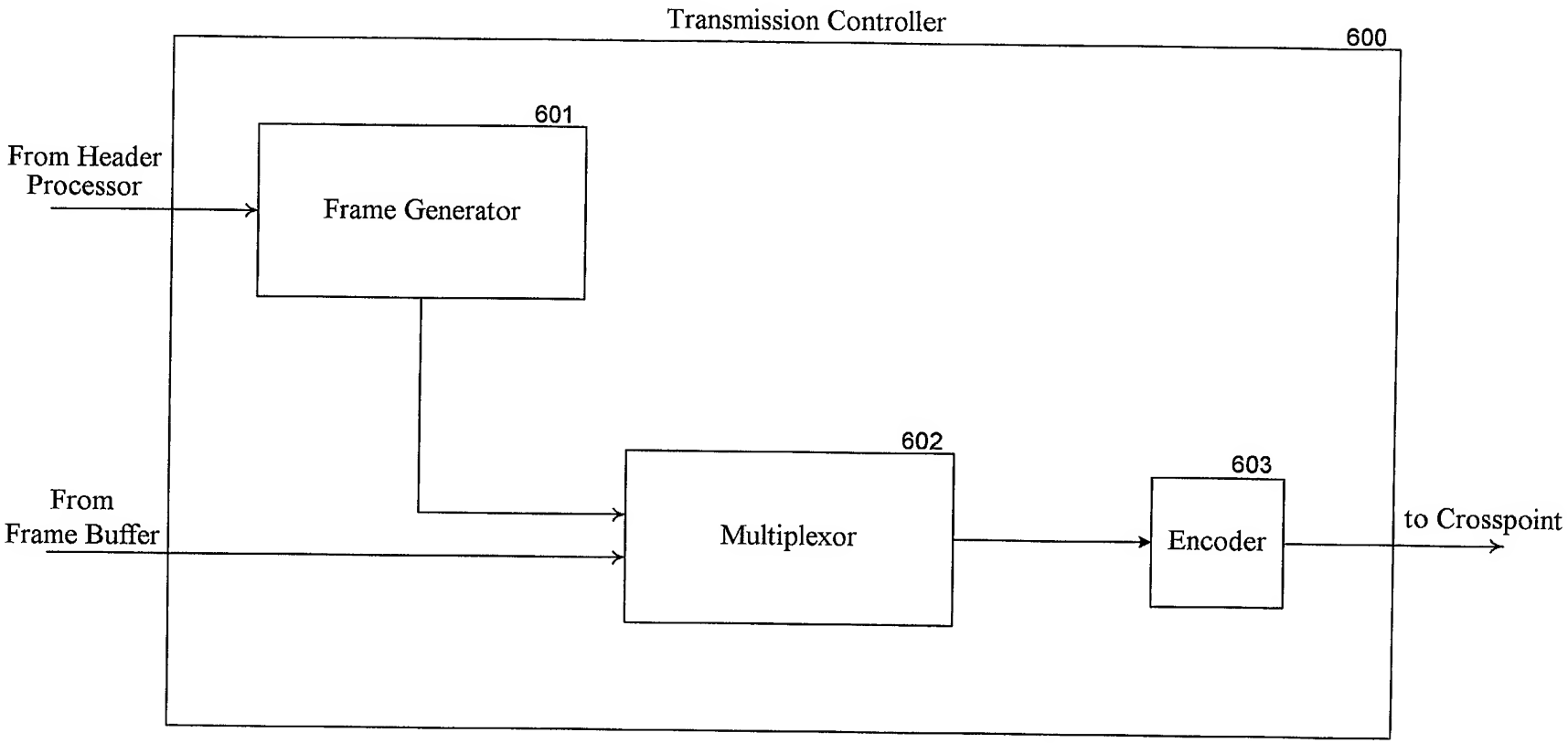

Transmission Controller
600
601
From Header Processor
Frame Generator
602
603
From Frame Buffer
Multiplexor
Encoder
to Crosspoint

Fig. 6

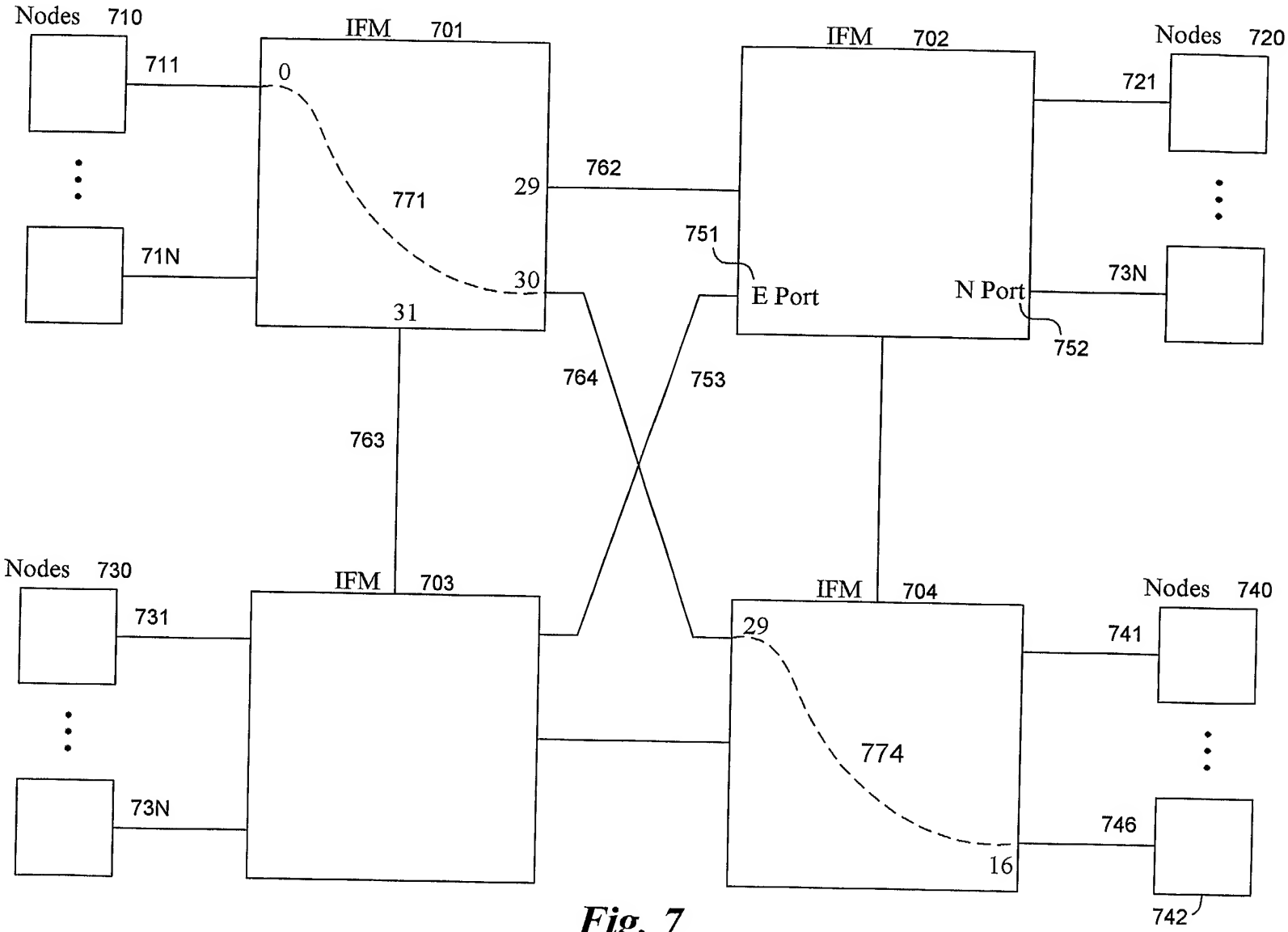

Nodes 710
711
71N
IFM 701
0
29
30
31
771
762
763
764
753
751
IFM 702
E Port
N Port
752
Nodes 720
721
73N
Nodes 730
731
73N
IFM 703
IFM 704
29
774
16
Nodes 740
741
746
742

Fig. 7

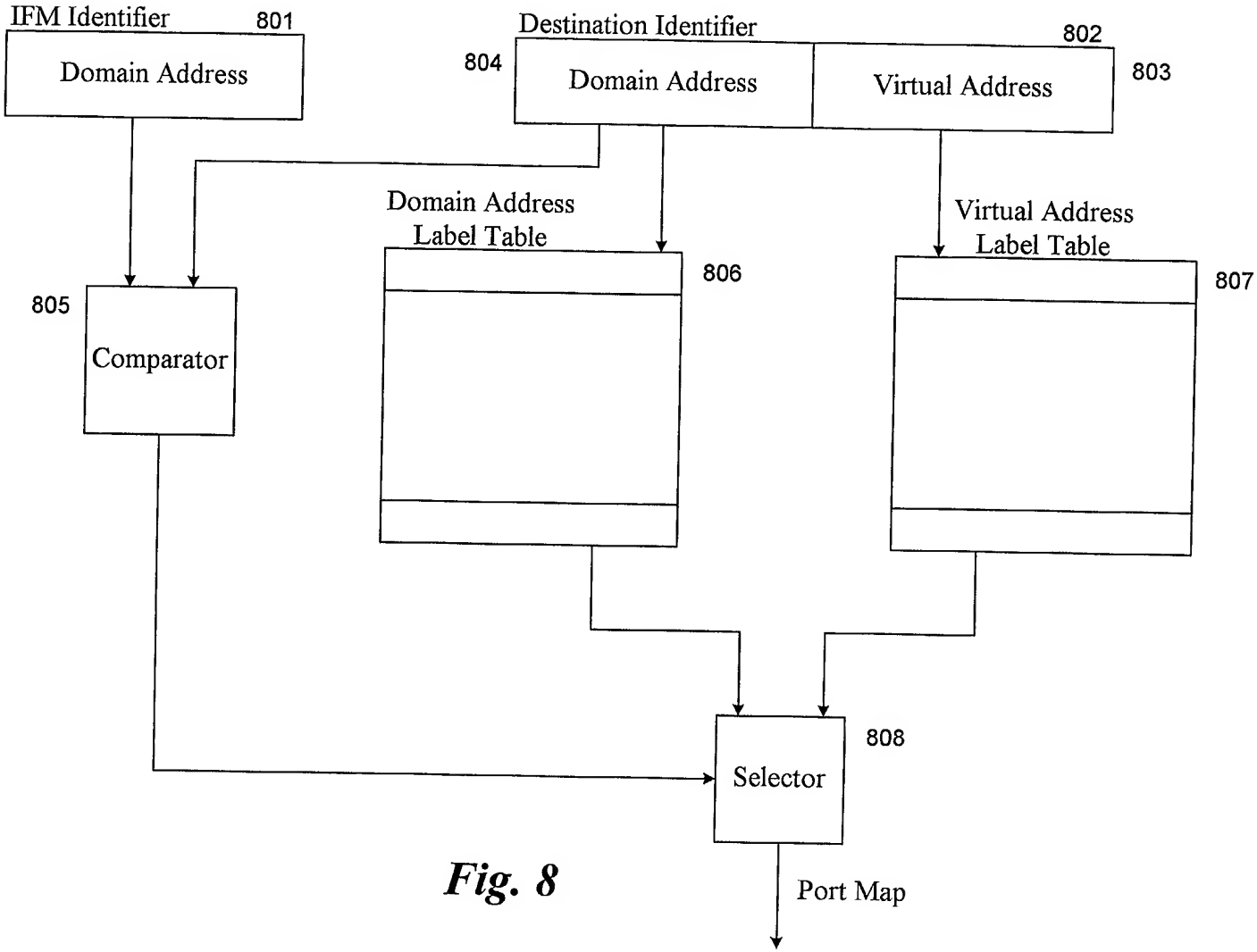

IFM Identifier
801
Domain Address
Destination Identifier
802
804
Domain Address
Virtual Address
803
Domain Address
Label Table
806
Virtual Address
Label Table
807
805
Comparator
808
Selector
Port Map

Fig. 8

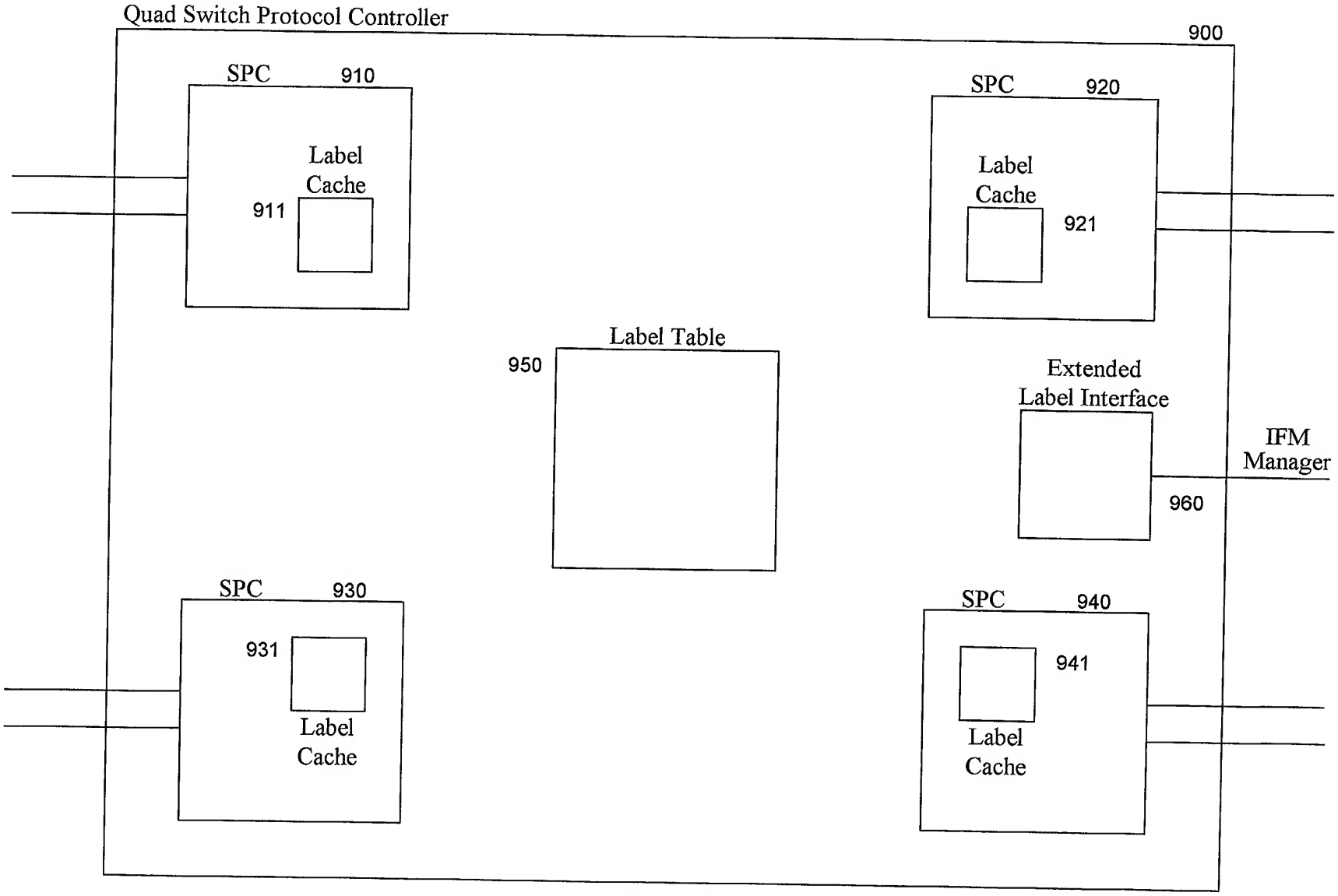

Quad Switch Protocol Controller
900
SPC
910
Label
Cache
911
SPC
920
Label
Cache
921
Label Table
950
Extended
Label Interface
960
IFM
Manager
SPC
930
931
Label
Cache
SPC
940
941
Label
Cache

Fig. 9

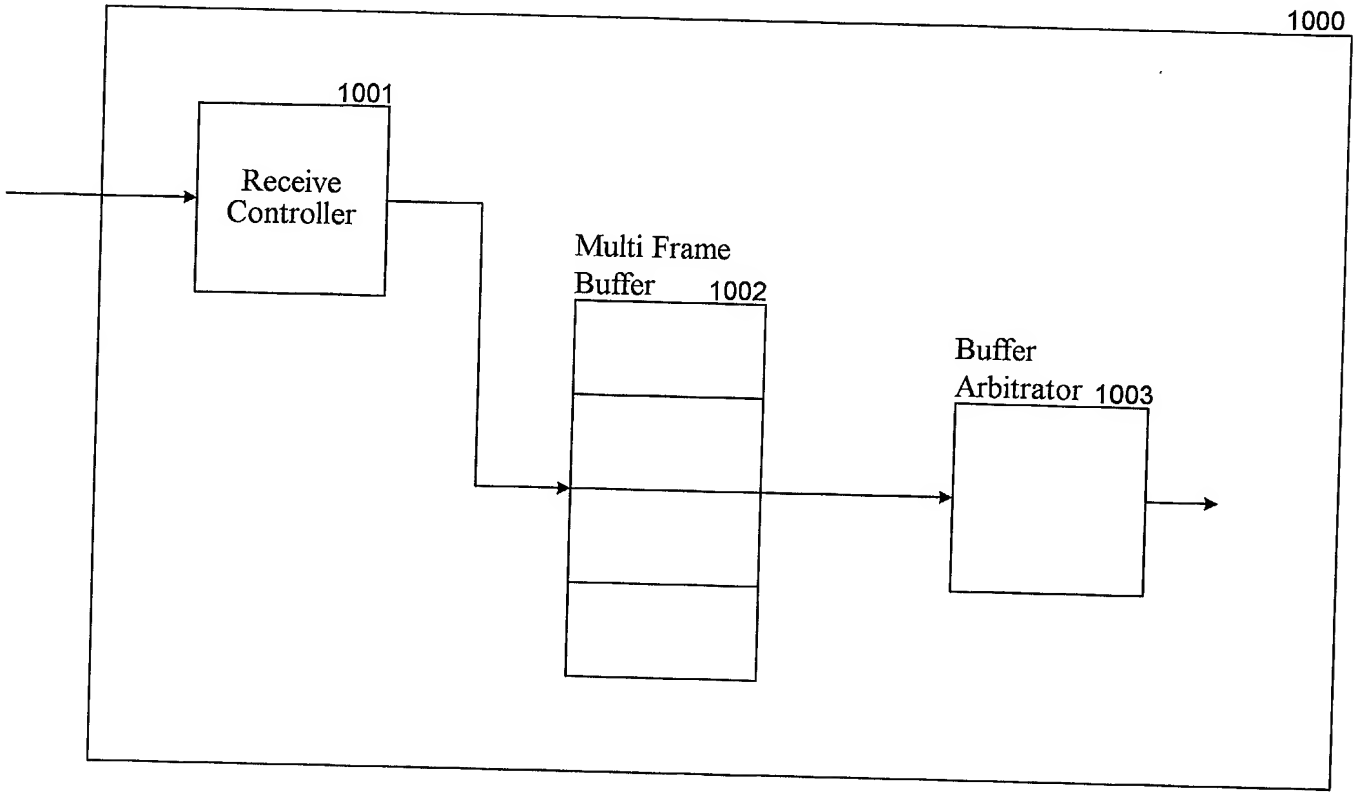

1000
1001
Receive Controller
Multi Frame Buffer
1002
Buffer Arbitrator
1003

Fig. 10

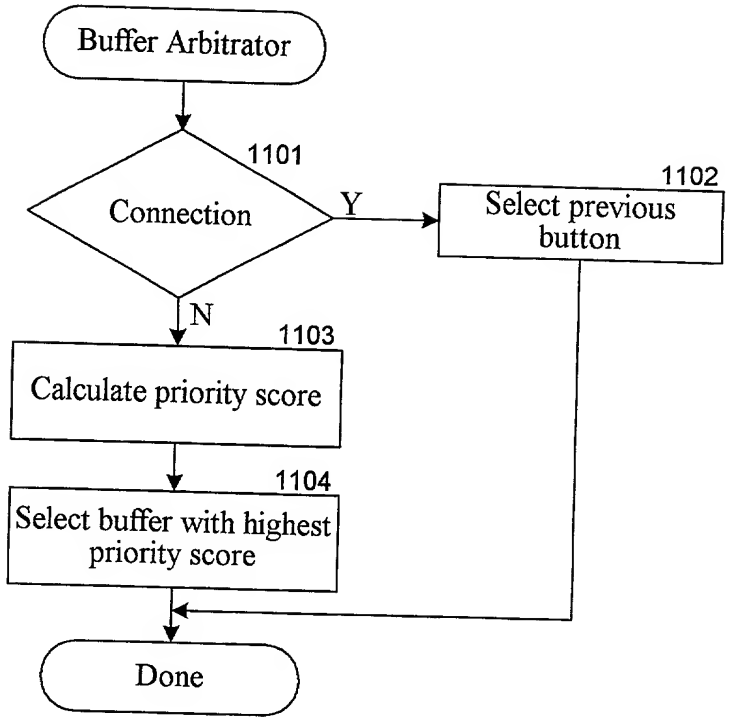

Buffer Arbitrator
1101
Connection
Y
1102
Select previous button
N
1103
Calculate priority score
1104
Select buffer with highest priority score
Done

Fig. 11

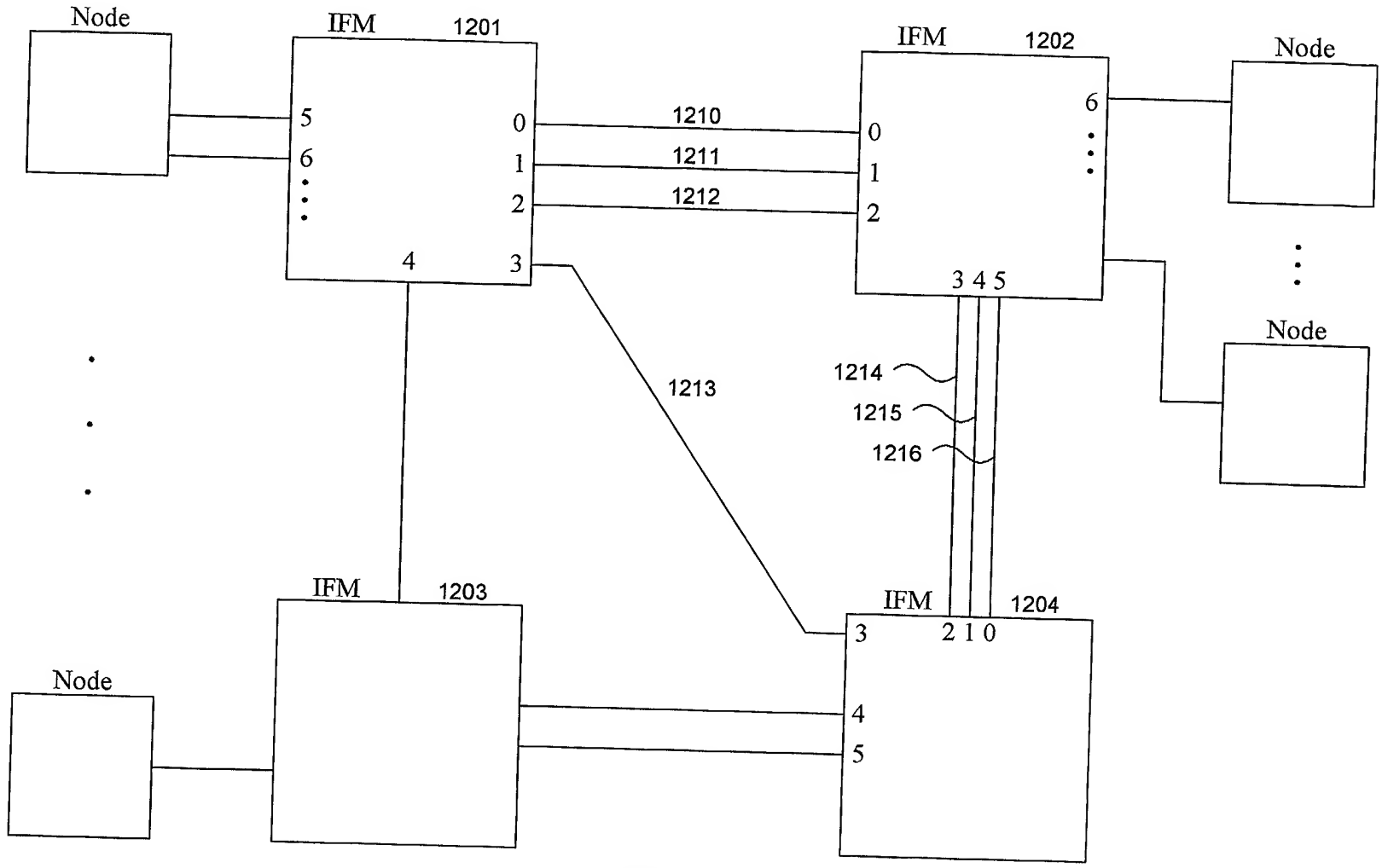

Node
IFM
1201
IFM
1202
Node
5
6
0
1
2
4
3
1210
1211
1212
0
1
2
6
3 4 5
1213
1214
1215
1216
Node
IFM
1203
IFM
1204
Node
3
2 1 0
4
5

Fig. 12

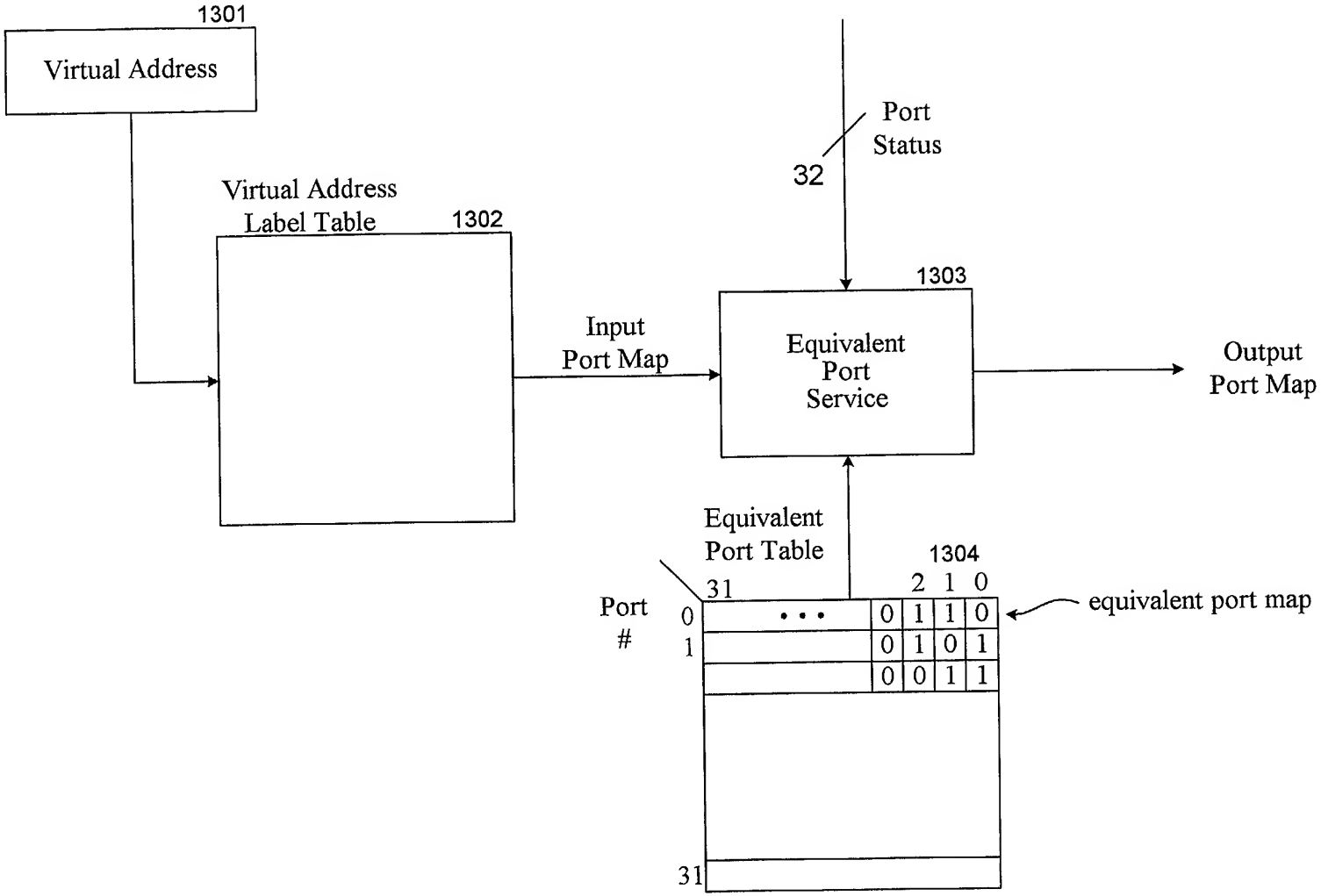

1301
Virtual Address
Virtual Address
Label Table
1302
Port
Status
32
1303
Input
Port Map
Equivalent
Port
Service
Output
Port Map
Equivalent
Port Table
1304
31
2 1 0
Port
#
0
1
equivalent port map
0 1 1 0
0 1 0 1
0 0 1 1
31

Fig. 13

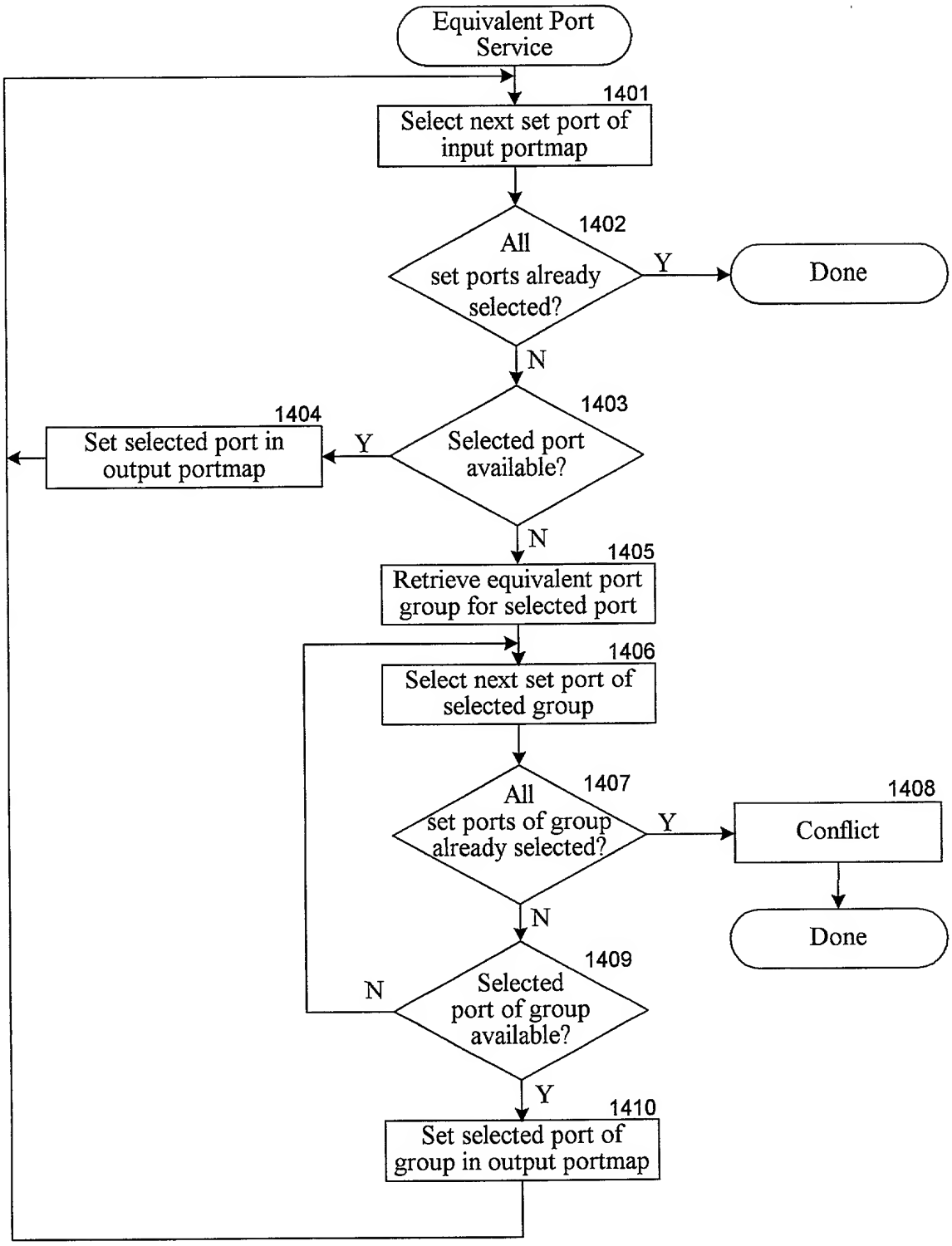

Equivalent Port Service
1401
Select next set port of input portmap
1402
All set ports already selected?
Y
Done
N
1403
Selected port available?
Y
1404
Set selected port in output portmap
N
1405
Retrieve equivalent port group for selected port
1406
Select next set port of selected group
1407
All set ports of group already selected?
Y
1408
Conflict
Done
N
1409
Selected port of group available?
N
Y
1410
Set selected port of group in output portmap

Fig. 14

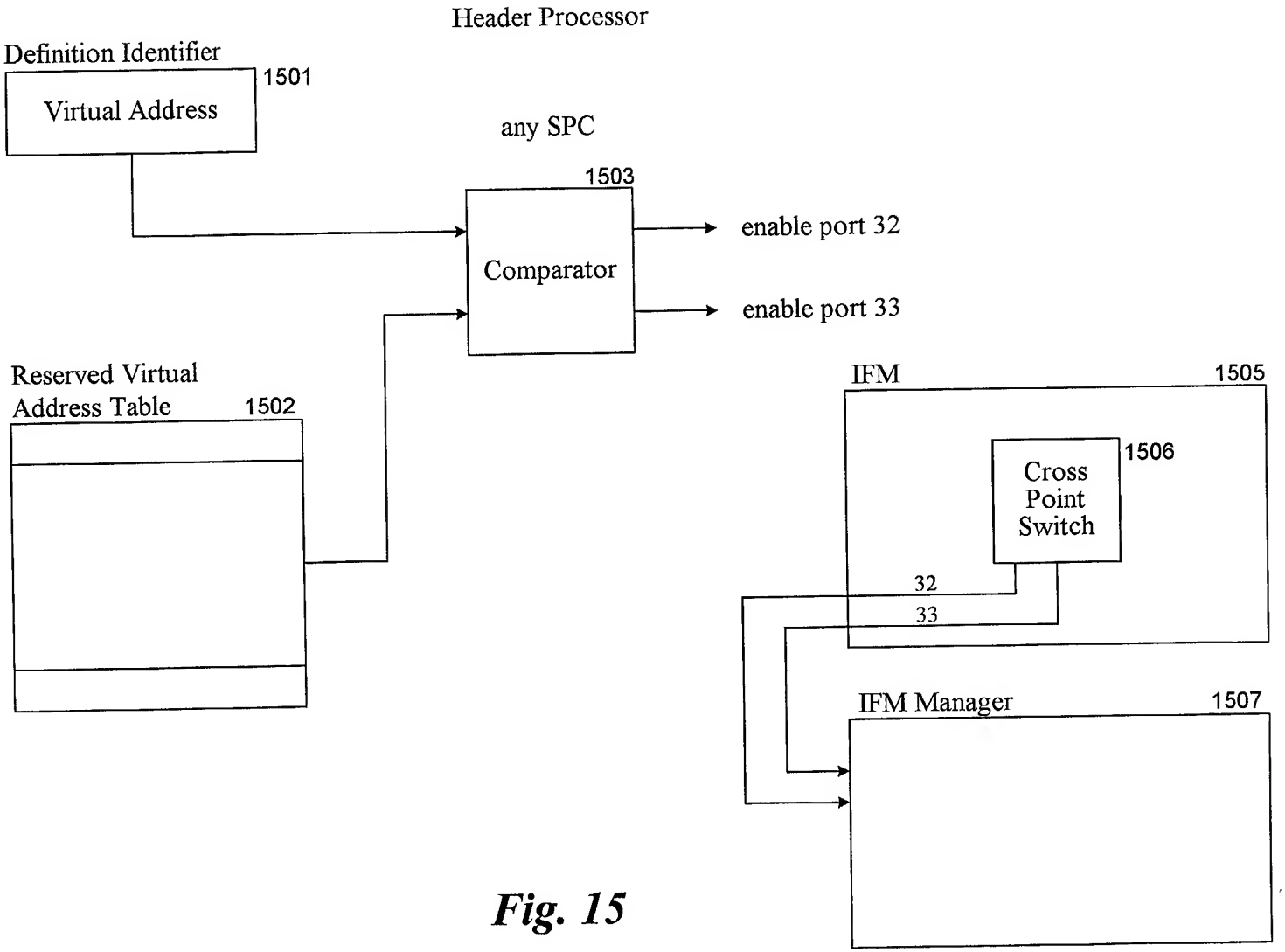
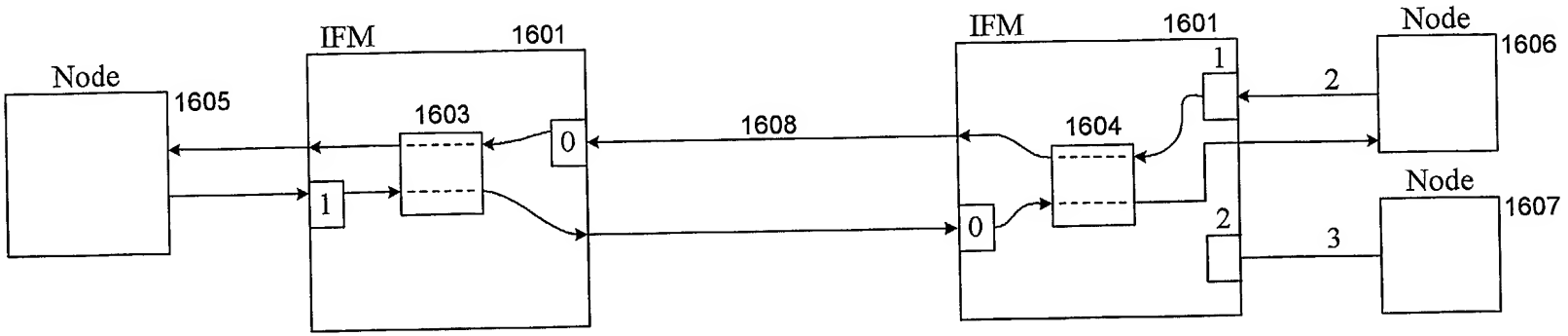

Header Processor
Definition Identifier
Virtual Address
1501
any SPC
1503
Comparator
enable port 32
enable port 33
Reserved Virtual
Address Table
1502
IFM
1505
Cross
Point
Switch
1506
32
33
IFM Manager
1507

Fig. 15



Time	Node 1605	IFM 1601	Node 1606	IFM 1602
0	Send start connect		Send start connect	
1		Connect 1↔0		Connect 2↔0
2		Forward start connect		Forward start connect
3		Can't forward start connect Node 1		Can't forward start connect

Fig. 16

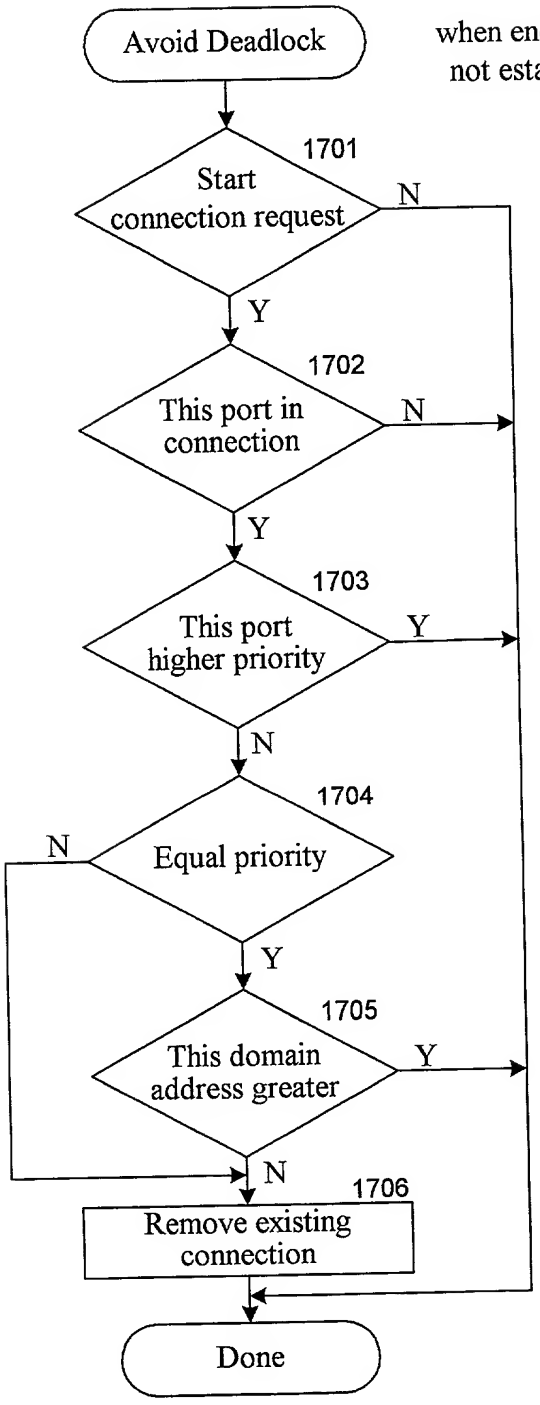

Avoid Deadlock
when end-to-end not established
1701
Start connection request
N
Y
1702
This port in connection
N
Y
1703
This port higher priority
Y
N
1704
Equal priority
N
Y
1705
This domain address greater
Y
N
1706
Remove existing connection
Done

Fig. 17

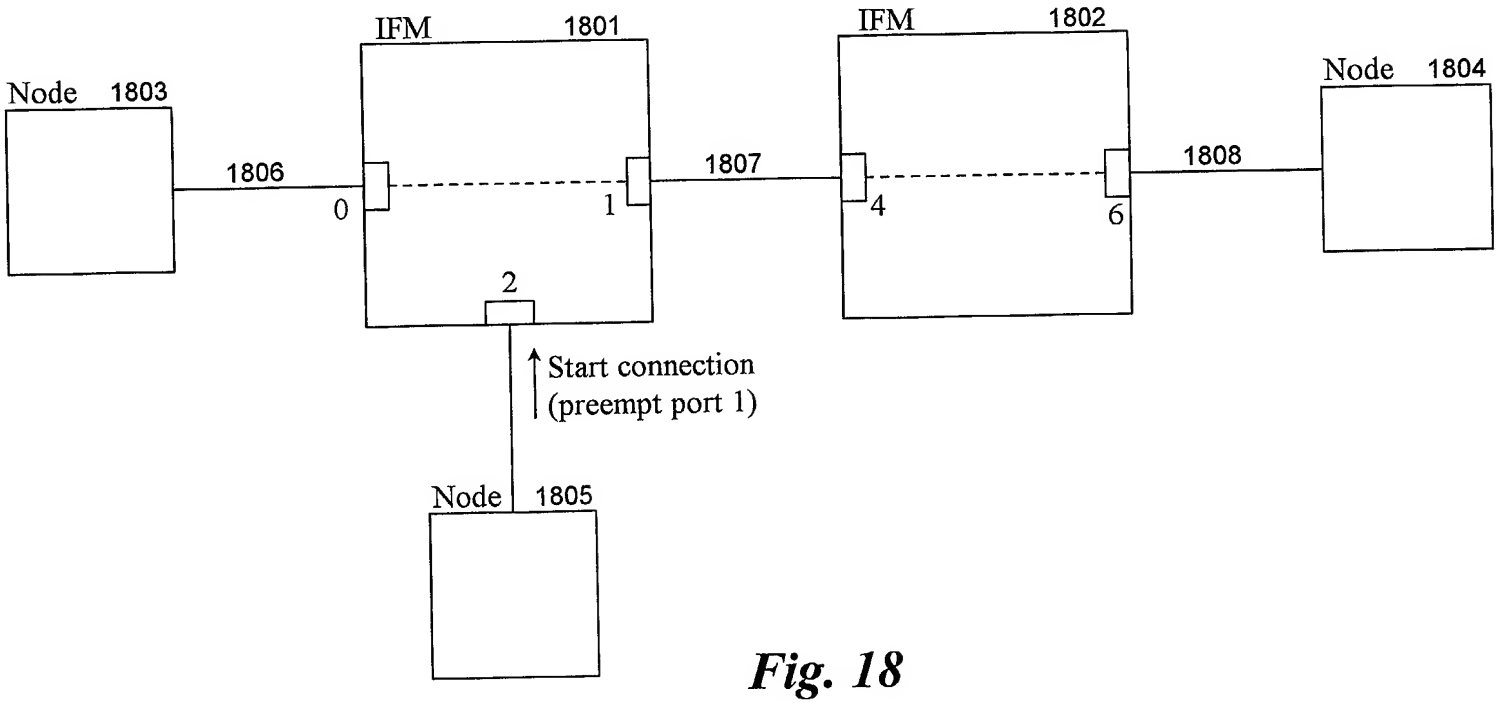

IFM
1801
IFM
1802
Node
1803
Node
1804
1806
1807
1808
0
1
4
6
2
Start connection
(preempt port 1)
Node
1805

Fig. 18

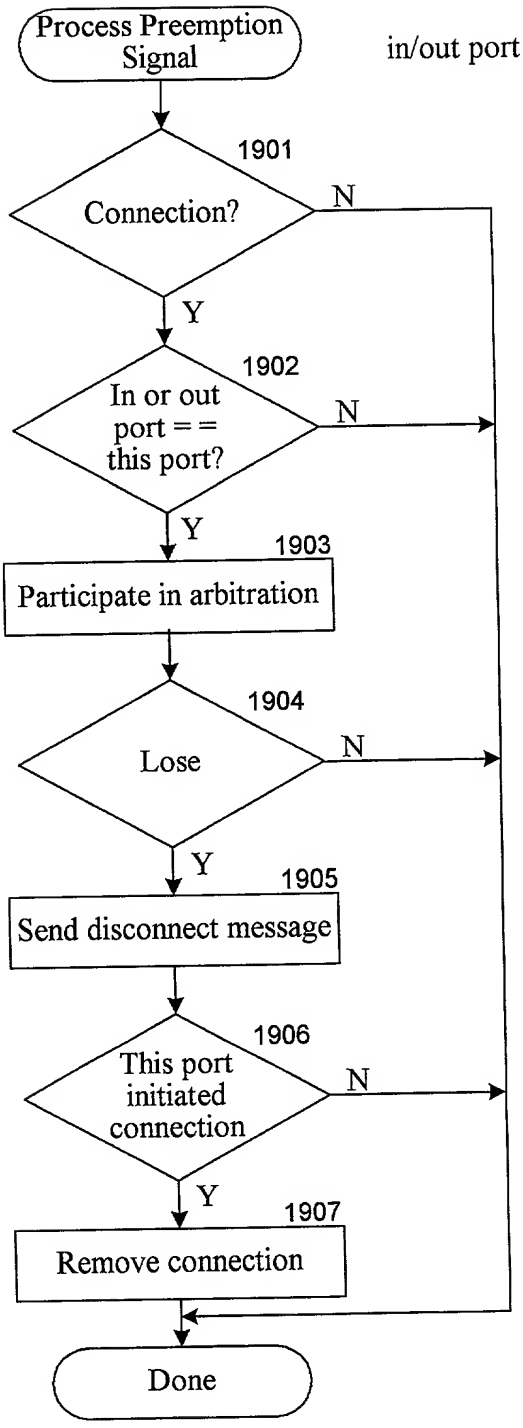

Process Preemption Signal
in/out port
1901
Connection?
N
Y
1902
In or out port = = this port?
N
Y
1903
Participate in arbitration
1904
Lose
N
Y
1905
Send disconnect message
1906
This port initiated connection
N
Y
1907
Remove connection
Done

Fig. 19

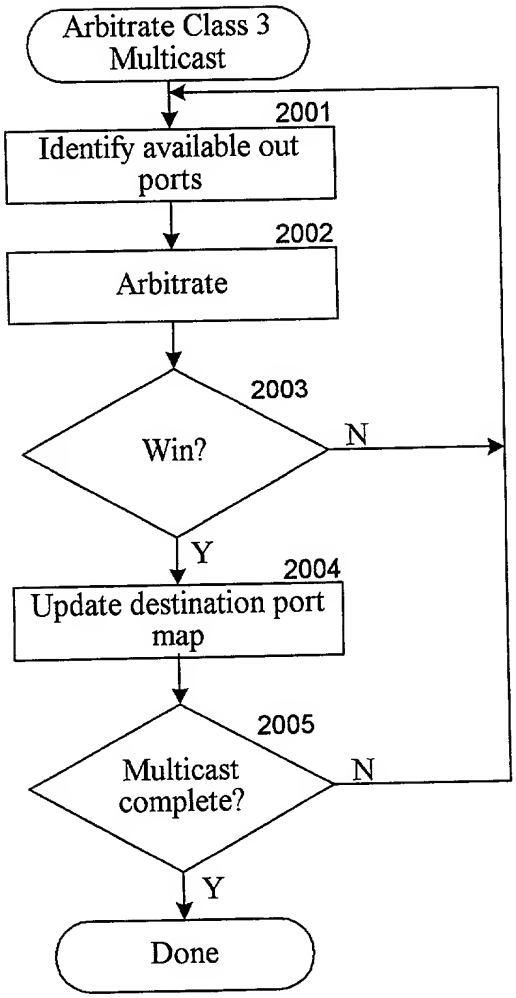

Arbitrate Class 3 Multicast
2001
Identify available out ports
2002
Arbitrate
2003
Win?
N
Y
2004
Update destination port map
2005
Multicast complete?
N
Y
Done

Fig. 20